



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

ne

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/354,302	07/16/1999	CHRISTOPHER K. MORZANO	M4065.0176/P	4970

24998 7590 05/22/2002

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L STREET NW
WASHINGTON, DC 20037-1526

EXAMINER

LUU, AN T

ART UNIT

PAPER NUMBER

2816

DATE MAILED: 05/22/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/354,302	MORZANO, CHRISTOPHER K.	
	Examiner An T. Luu	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 11 March 2002.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-56 and 82-98 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) 38-56 is/are allowed.
- 6) Claim(s) 1-8,11-20,23-33,36,37 and 82-98 is/are rejected.
- 7) Claim(s) 9,10,21,22,34,35 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

<ol style="list-style-type: none"> 1) <input type="checkbox"/> Notice of References Cited (PTO-892) 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____. 	<ol style="list-style-type: none"> 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____. 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) 6) <input type="checkbox"/> Other: _____.
---	---

DETAILED ACTION

Applicant's Response filed on 3-11-02 has been received and entered in the case. The rejections set forth in the previous Office Action are maintained as indicated below.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-7, 16-19, 82 and 86-90 are rejected under 35 U.S.C. 102(b) as being anticipated by the Makihara et al. (U.S. Patent 5,243,573).

Makihara et al discloses in figure 2 an apparatus comprising a first and second complementary clock signal input/output lines (line connecting N4 and transistor 29, and N5 and transistor 30) for receiving first and second complementary clock input signals and transmitting first and second complementary clock input signals (at nodes N4 and N5 by virtue of a latch made up by transistors 24-27); first (24,26) and second (25,27) inverters each having an input and an output, wherein the input of the first inverter connected to the output of the second inverter and to the first clock signal input/output line and the input of the second inverter connected to the output of the first inverter and to the second clock signal input/output line as required by claim 1.

As to claim 2, figure 2 shows an enable circuit (12 and 17) for receiving an enable signal and enabling or disabling the first and second inverters in response to the enable signal (SE, /SE).

As to claims 3-5, figure 2 shows a first voltage source (+V) coupled to the first and second inverters by means of enable signal (/SE) via P-channel transistor 12; and a second voltage source (GRD) coupled to the first and second inverters by means of the inverted enable signal (SE) via N-channel transistor. It is inherent that there exists an enable inverter for inverting the enable signal since SE and /SE are complementary signal. For simplicity, the enable inverter is not shown in the figure.

As to claims 6-7, the scopes of these claims are similar to those of claims 4 and 5. It is noted that the first and second voltages are Ground and V+, respectively.

As to claims 14-15, these claims recite a structure as shown in figure 3 of the instant application. These claims are rejected since transistor 24-27, 12 and 17 in figure 2 of Makihara are configured exactly as required by the claims (fig 3 of Applicant).

The scopes of claims 16-19 are similar to those of claims 3-7 and 15. Therefore, they are rejected for the similar reasons set forth above.

Claims 82 and 86-90 are rejected as being directed to the method or/and steps derived from the apparatus described in claims 1-8 and 16-19 noted above.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 8, 11-13, 20, 23-33, 36-37, 83-85 and 91-98 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Makihara et al. (U.S. Patent 5,243,573) in view of the Garcia reference (5,949,259).

Makihara et al discloses all the claimed limitations except for having a first and second buffer or driver circuits coupled to the first and second complementary clock signal input/output lines as required by claims 8, 11 and 20. First, it is noted that buffer and driver have the same meaning in the field of electrical circuitry. Secondly and lastly, Official Notice is taken for the fact that a driver circuit coupling to a signal line. It is notoriously well known in the art that a driver circuit is used for re-shaping (i.e., delaying, amplifying) a signal to a particular desired form suitable for further processing. Therefore, it would have been obvious to one skilled in the art to incorporate a driver circuit into the input/output line taught by Makihara et al to achieve a desirable form of signal that meets the requirement of a particular application.

As to claims 12 and 13, the Garcia reference discloses in figure 6 a driver circuit comprising at least a first and a second driver inverter (202; P4 and N4) connected in series as required by claim 12; and a third inverter (P2,N3) wherein the third inverter and the series connected inverters have the same input and the output of the third inverter connected to a device N1 such that the output of the series connected inverters is set to a predetermined voltage (Vo). It would have been obvious for one skilled in the art to select a driver circuit taught by Garcia because the skilled artisans will easily recognize that a driver circuit can be implemented in many different ways in the art, one of such way is as shown in the Garcia for controlling a slew-rate of an output buffer circuit. Selecting one of the known designs is seen as design expedient

depending upon the particular requirement of the application. Such a selection would improve the teaching of Makihara without departing from the scope and spirit of his invention.

The scopes of claims 23-25 are similar to those of claims 11-13. Therefore, they are rejected for the similar reasons set forth above.

The scopes of claims 26 and 27-33 are similar to those of claims 11 and 2-8, respectively. Therefore, they are rejected for the similar reasons set forth above.

The scopes of claims 36-37 are similar to those of claims 12-13. Therefore, they are rejected for the similar reason set forth above.

Claims 83-85 and 91-98 are rejected as being directed to the method or/and steps derived from the apparatus described in claims 8, 11-13 and 23-33 noted above.

Response to Arguments

5. Applicant's arguments filed 3-11-02 have been fully considered but they are not persuasive.

Regarding to the rejection of independent claims 1, 16 and 82 under 35 USC 102 by Makihara, Applicant has argued that (1) Makihara's invention does not receive complementary clock signals as input signals nor does it output complementary clock signals; and (2) the skew of the signals [in Makihara's invention] would not be reduced. Examiner respectfully disagrees on the first assertion because transistors 24-27 are configured as two inverters in anti-parallel. Therefore, their input/output signals are complementary signals. It is irrelevant to response to the second assertion since it is not recited in claims.

Regarding to the rejection of claims 8, 11-13, 20, 23-33, 36-37, 83-85 and 91-98 under 35 USC 103 by Makihara in view of Garcia, Applicant has argued that Garcia's circuit does not receive input/output complementary signals. Examiner respectfully disagrees with the above assertion because Garcia is a secondary reference for showing a buffer coupled the input/output. Therefore, complementary signals are not necessarily required to be taught by Garcia.

Allowable Subject Matter

6. Claims 38-56 are allowed.
7. Claims 9-10, 21-22 and 34-35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
8. The following is a statement of reasons for the indication of allowable subject matter: see the previous Office Action.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

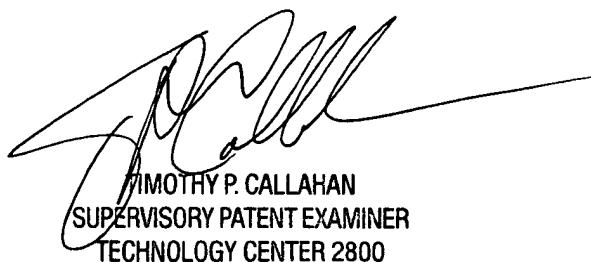
10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to An T. Luu whose telephone number is 703-308-4922. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

An T. Luu

5-16-02



TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800